

Deming Chen

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Education

Ph. D.	University of California, Los Angeles, 2005
M. S. Computer Science	University of California, Los Angeles, 2001
B. S. Computer Science	University of Pittsburgh, Pittsburgh, 1995
B. S. Physical Chemistry	Amoy (Xiamen) University, Xiamen, China, 1990

Research Interests

- Nanotechnology-centric FPGA architecture and CAD
- Microprocessor architecture and CAD under parameter variation
- CAD for programmable logic devices
- Behavioral synthesis
- Low power design and synthesis
- Reconfigurable computing
- Application-specific processor design
- Algorithmic design and applications

Work Experience

Aug. 2005 – Present	Assistant Professor Department of Electrical and Computer Engineering University of Illinois, Urbana-Champaign
Aug 2000 – Aug. 2005	Graduate Research Assistant Computer Science Department University of California, Los Angeles
Mar 2001 – Jul 2002	Software Engineer Aplus Design Technologies, Inc. Los Angeles, California
Jul 1995 – Sep 1999	System Engineer Applied Systems Associates, Inc. Murrysville, Pennsylvania
Sep 1990 – Sep 1991	Research Staff Institute of Coal Chemistry Chinese Academy of Sciences, China

Teaching Experience

- Spring 2008/2009, ECE 412: Microcomputer Laboratory
- Spring 2006, 2007, 2009, ECE 425: Introduction to VLSI System Design
- Fall 2006/2007, ECE 598BL: Design and Synthesis of System-on-a-chip (new course developed)
- Fall 2008/2009, ECE 527: System-on-Chip Design (permanent version of ECE 598BL above)

Awards and Honors

- Achievement Award for Excellent Teamwork, Aplus Design Technologies, Inc, 2001
- “Power Modeling and Characteristics of Field Programmable Gate Arrays” – one of the most-downloaded article from IEEE Transactions on CAD, 2006
- Strathmore’s Who’s Who, 2007-2008
- Arnold O. Beckman Research Award, UIUC, 2007
- NSF Career Award, 2008
- Included in the List of Teachers Ranked as Excellent, Spring 2008
- Best Paper Award, IEEE/ACM Asia and South Pacific Design Automation Conference, 2009
- Best Paper Award, IEEE Symposium on Application Specific Processors, 2009

Research Grants and Contracts

- Equipment grant, Intel, equivalent to \$20,000, 2005
- Software donation, Microsoft, \$3,000, 2005
- FPGA board and software donation, Altera, equivalent to \$41,000, 2006
- Research gift, Altera, \$20,000, (PI: Chen portion=\$10,000), 2006
- SRC, \$360,000, (co-PI, Chen portion=\$180,000), 2007-2010
- Research gift, Altera, \$15,000, (PI, Chen portion=\$7,500), 2007
- NSF, \$1,200,000, (co-PI, Chen portion=\$386,298), 2007-2010
- FPGA board and software donation, Xilinx, equivalent to \$18,500, 2007, 2009
- NSF, \$400,000, CAREER Grant, 2008-2013
- Research gift, UIUC research board, (co-PI, Chen portion=\$5,964), 2008
- Research gift, Altera, \$20,000, (PI, Chen portion=\$10,000), 2008
- Research gift, Sun Microsystems, \$23,000, 2008-2010
- Intel Undergraduate Research Program (ISUR), \$2,200, 2009-2010
- MARCO/DARPA Gigascale System Research Center, \$236,400, 2009-2012

Instruction Grants and Donations

- FPGA board donation (30 DE2 educational boards), Altera, 2006
- Quartus II design environment and Nios II embedded soft processors (30 licenses), Altera, 2006
- TRDB_DC2 1.3Mega Pixel Digital Camera Module (30 items), Altera, 2006

Professional Activities and Services

Editorship:

- Associate editor, VLSI Circuit and Semiconductor Technology Division, Translated Series on Foreign Advanced Technologies, China Machine Press, 2007
- Associate editor, ACM SIGDA Electronic Newsletter, 2008 – present
- Associate editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009 – present
- Associate editor, Journal of Low Power Electronics (JOLPE), 2009 – present
- Associate editor, Journal of Circuits, Systems and Computers (JCSC), 2009 – present

Service to Professional Conferences:

Various chair positions

- Technical program subcommittee chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2009, 2010
- CAD track co-chair, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- Session chair, IEEE International Conference on Computer Design (ICCD), 2005
- Session chair, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007
- Session chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2007, 2008
- Session chair, ACM/SIGDA International Symposium on FPGA (FPGA), 2008
- Session organizer, IEEE/ACM Design Automation Conference (DAC), 2009
- Session chair, Design, Automation and Test in Europe (DATE), 2009
- Session chair, IEEE System Level Interconnect Prediction (SLIP), 2009
- CAD track co-chair, IEEE International Symposium on Circuits and Systems (ISCAS), 2010

Technical program committee member

- ACM/SIGDA International Symposium on FPGA (FPGA), 2006-2010
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2007-2010
- IEEE International Symposium on Circuits and Systems (ISCAS), 2007-2008
- IEEE International Conference on Computer Design (ICCD), 2007-2009
- International Conference on Field Programmable Logic and Applications (FPL), 2008-2009
- IEEE/ACM International Symposium on Quality Electronic Design (ISQED), 2009-2010
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2009-2010
- IEEE Reconfigurable Architectures Workshop (RAW), 2009-2010
- IEEE/ACM Design Automation Conference (DAC), 2009-2010
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2009
- IEEE Symposium on Application Specific Processors (SASP), 2009
- IEEE System Level Interconnect Prediction (SLIP), 2009
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2009
- International Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA), 2009
- ACM/SIGDA Ph.D. Forum at DAC, 2007-2009
- IEEE International Conference on VLSI Design, 2010
- Design, Automation, and Test in Europe (DATE), 2010

Panel/workshop organizer

- Workshop co-organizer and co-coordinator: “Grand Challenges in FPGA Research”, 2007

- Panel co-chair and moderator: “CMOS vs. NANO: Comrades or Rivals,” ACM/SIGDA International Symposium on FPGA, 2009
- Panel organizer and moderator, "Impact of Emerging Interconnect Technologies on SLIP Research Directions", IEEE System Level Interconnect Prediction (SLIP), 2009

Tutorial and Panelist

- Panelist: “Best ways to Use Billions of Devices on a Chip,” IEEE/ACM Asia and South Pacific Design Automation Conference, 2008
- Tutorial presenter: “Latest Advances and Future Opportunities on CAD for FPGAs,” IEEE/ACM Asia and South Pacific Design Automation Conference, 2008
- Tutorial organizer and presenter: “From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials,” IEEE/ACM Design Automation Conference, 2009

Proposal Review

- External proposal reviewer, Natural Sciences and Engineering, Research Council of Canada, 2008, 2009
- External proposal reviewer, Israel Science Foundation, 2008
- External research proposal reviewer, Qatar National Research Fund, 2009

Journal Review

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Advanced Packaging (TAP)
- ACM Transactions on Reconfigurable Technology and Systems (TRETs)
- IEEE Transactions on Nanotechnology (TN)
- Integration, the VLSI Journal
- Journal of Low Power Electronics (JOLPE)
- IET Circuits, Devices & Systems

Student Advising

Graduate Students:

- Christine Chen, Ph.D.
- Scott Chilstedt, Ph.D.
- Quang Dinh, Ph.D.
- Chen Dong, Ph.D.
- Greg Lucas, Ph.D.
- Alex Papakonstantinou, Ph.D.
- Chi-Chen Peng, M.S.
- Lu Wan, Ph.D.

Visiting Scholar:

- Chun (Cerelia) He (China Scholarship Council)
- Su (Sherry) Liu (China Scholarship Council)

Undergraduate Researchers:

- Yohannes Kifle (Intel Undergraduate Scholar)
- Artem Rogachev

Alumni:

- Shoaib Akram, M.S., 2009
- Scott Cromar, M.S., 2009
- Lei Cheng (co-advised with Prof. Martin Wong), Ph.D., 2007 (joined Synplicity)
- Allyson Moisan, Undergraduate Researcher
- Jaeho Lee, Undergraduate Researcher

Publications

Book Chapters

B1. D. Chen, Chapter 38: Design Automation for Microelectronics, *Handbook of Automation*, Springer Publishers, to appear.

Journal Papers

- J1. D. Chen, J. Cong, Y. Fan, and L. Wan, "LOPASS: A Low-Power Architectural Synthesis System for FPGAs with Interconnect Estimation and Optimization", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, to appear.
- J2. S. Chilstedt, C. Dong, and D. Chen, "Design and Evaluation of a Carbon Nanotube-Based Programmable Architecture", *International Journal of Parallel Programming (IJPP), Special Issue on Nano/Bio-Inspired Applications, Architectures and Software*, Vol. 37, Issue 4, pp. 389-416, Aug. 2009.
- J3. H. Li, D. H. Kwon, D. Chen, and Y. Chiu, "A Fast Digital Predistortion Algorithm for Radio-Frequency Power Amplifier Linearization with Loop Delay Compensation," *IEEE Journal of Selected Topics in Signal Processing, Special Issue on: DSP Techniques for RF/Analog Circuit Impairments*, Vol. 3, No. 3, pp.374-383, June 2009.
- J4. L. Cheng, D. Chen, and D.F. Wong, "DDBDD: Delay-Driven BDD Synthesis for FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 27, No. 7, pp.1203-1213, July 2008.
- J5. L. Cheng, D. Chen and M. Wong, "A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 13, No. 2, Article 34, Apr. 2008.
- J6. C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, "3D nFPGA: A Reconfigurable Architecture for 3D CMOS/Nanomaterial Hybrid Digital Circuits," *IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications*, Vol. 54, Issue 11, pp. 2489-2501, November 2007.
- J7. D. Chen, J. Cong, and P. Pan, "FPGA Design Automation: A Survey," *Foundations and Trends in Electronic Design Automation*, Vol. 1, No 3, 195-330, November 2006.

- J8. D. Chen, J. Cong, and J. Xu, "Optimal Simultaneous Module and Multi-Voltage Assignment for Low-Power," *ACM Transactions on Design Automation of Electronic Systems*, vol. 11, Issue 2, pp. 362-386, April 2006.
- J9. F. Li, Y. Lin, L. He, D. Chen, and J. Cong, "Power Modeling and Characteristics of Field Programmable Gate Arrays," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, Issue 11, pp. 1712-1724, November 2005.
- J10. D. Chen, J. Cong, M. Ercegovac, and Z. Huang, "Performance-Driven Mapping for CPLD Architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 10, pp. 1424-1431, October 2003.

Conference Papers

- C1. L. Wan and D. Chen, "DynaTune: Circuit-Level Optimization for Timing Speculation Considering Dynamic Path Behavior", *IEEE/ACM International Conference on Computer-Aided Design*, Nov. 2009.
- C2. C. He, A. Papakonstantinou, and D. Chen, "A Novel SoC Architecture on FPGA for Ultra Fast Face Detection", *IEEE International Conference on Computer Design*, Oct. 2009.
- C3. S. Akram, R. Kumar, and D. Chen, "Workload Adaptive Shared Memory Multicore Processors with Reconfigurable Interconnects," *IEEE Symposium on Application Specific Processors*, July 2009.
- C4. A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "FCUDA: Enabling Efficient Compilation of CUDA Kernels onto FPGAs," *IEEE Symposium on Application Specific Processors*, July 2009 (**Best Paper Award**).
- C5. S. Cromar, J. Lee, and D. Chen, "FPGA-Targeted High-Level Binding Algorithm for Power and Area Reduction with Glitch-Estimation," *IEEE/ACM Design Automation Conference*, July 2009.
- C6. C. Dong, S. Chilstedt, and D. Chen, "Variation Aware Routing for Three-Dimensional FPGAs," *IEEE Computer Society Annual Symposium on VLSI*, May 2009.
- C7. C. Dong, S. Chilstedt, and D. Chen, "Reconfigurable Circuit Design with Nanomaterials," *Design, Automation and Test in Europe*, Apr. 2009. (**Invited**)
- C8. Q. Dinh, D. Chen, and D.F. Wong, "A Routing Approach to Reduce Glitches in Low Power FPGAs," *IEEE/ACM International Symposium on Physical Design*, March 2009.
- C9. C. Dong, S. Chilstedt, and D. Chen, "FPCNA: Field Programmable Carbon Nanotube Array," *ACM/SIGDA International Symposium on FPGA*, Feb. 2009.
- C10. B. Greskamp, L. Wan, R. Karpuzcu, J. Cook, J. Torrellas, D. Chen, and C. Zilles "BlueShift: Designing Processors for Timing Speculation from the Ground Up," *IEEE International Symposium on High-Performance Computer Architecture*, Feb. 2009.
- C11. G. Lucas, S. Cromar, and D. Chen, "FastYield: Variation-Aware, Layout-Driven Simultaneous Binding and Module Selection for Performance Yield Optimization," *IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2009 (**Best Paper Award**).
- C12. A. Papakonstantinou, Y. Kifle, G. Lucas, and D. Chen, "MP3 decoding on FPGA: A case study for floating point acceleration," *Proceedings of Reconfigurable Systems Summer Institute*, Urbana, IL, July 2008.

- C13. A. Papakonstantinou, D. Chen, and W.M. Hwu, "Application Acceleration with the Explicitly Parallel Operations System – the EPOS Processor," *IEEE Symposium on Application Specific Processors*, June 2008.
- C14. Q. Dinh, D. Chen, and D.F. Wong, "Efficient ASIP Design for Configurable Processors with Fine-Grained Resource Sharing," *ACM/SIGDA International Symposium on FPGA*, February 2008.
- C15. S. Akram, S. Cromar, G. Lucas, A. Papakonstantinou, and D. Chen, "VEBoC: Variation and Error-Aware Design for Billions of Devices on a Chip," *IEEE/ACM Asia and South Pacific Design Automation Conference*, January 2008. **(Invited)**
- C16. L. Cheng, D. Chen, D.F. Wong, M. Hutton, and J. Govig, "Timing Constraint-driven Technology Mapping for FPGAs Considering False Paths and Multi-Clock Domains," *IEEE/ACM International Conference on Computer-Aided Design*, Nov. 2007.
- C17. C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, "Performance and Power Evaluation of a 3D CMOS/Nanomaterial Reconfigurable Architecture," *IEEE/ACM International Conference on Computer-Aided Design*, Nov. 2007.
- C18. Q. Dinh, Y. Bresler, and D. Chen, "Hardware Acceleration for Sparse Fourier Image Reconstruction," *IEEE International Conference on ASIC*, Oct. 2007. **(Invited)**
- C19. L. Cheng, D. Chen, and D.F. Wong, "GlitchMap: An FPGA Technology Mapper for Low Power Considering Glitches," *IEEE/ACM Design Automation Conference*, Jun. 2007.
- C20. L. Cheng, D. Chen, and D.F. Wong, "DDBDD: Delay-Driven BDD Synthesis for FPGAs," *IEEE/ACM Design Automation Conference*, Jun. 2007.
- C21. D. Chen, J. Cong, Y. Fan, and Z. Zhang, "High-Level Power Estimation and Low-Power Design Space Exploration for FPGAs," *IEEE/ACM Asia and South Pacific Design Automation Conference*, Japan, January 2007.
- C22. L. Cheng, L. Deng, D. Chen, and D.F. Wong, "A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for Leakage Power Reduction," *IEEE/ACM Design Automation Conference*, July 2006.
- C23. J. Lin, D. Chen, and J. Cong, "Optimal Simultaneous Mapping and Clustering for FPGA Delay Optimization," *IEEE/ACM Design Automation Conference*, San Francisco, July 2006.
- C24. D. Chen, J. Cong, Y. Fan, and J. Xu, "Optimality Study of Resource Binding with Multi-Vdds," *IEEE/ACM Design Automation Conference*, San Francisco, July 2006.
- C25. D. Chen, J. Cong, Y. Fan, G. Han, W. Jiang, and Z. Zhang, "xPilot: A Platform-Based Behavioral Synthesis System," *Proceedings of SRC Techcon Conference*, October 2005.
- C26. D. Chen, J. Cong, and J. Xu, "Optimal Module and Voltage Assignment for Low-Power," *IEEE/ACM Asia and South Pacific Design Automation Conference*, Shanghai, China, January 2005.
- C27. D. Chen and J. Cong, "DAOmap: A Depth-Optimal Area Optimization Mapping Algorithm for FPGA Designs," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, California, pp. 752-759, November 2004.
- C28. D. Chen and J. Cong, "Delay Optimal Low-Power Circuit Clustering for FPGAs with Dual Supply Voltages," *IEEE/ACM International Symposium on Low Power Electronics and Design*, Newport Beach, California, pp. 70-73, August 2004.
- C29. D. Chen, J. Cong, F. Li, and L. He, "Low-Power Technology Mapping for FPGA Architectures with Dual Supply Voltages," *ACM/SIGDA International Symposium on FPGA*, Monterey, California, pp. 109-117, February 2004.

- C30. D. Chen and J. Cong, "Register Binding and Port Assignment for Multiplexer Optimization," *IEEE/ACM Asia and South Pacific Design Automation Conference*, Yokohama, Japan, pp. 68-73, January 2004.
- C31. D. Chen, J. Cong, and Y. Fan, "Low-Power High-Level Synthesis for FPGA Architectures," *IEEE/ACM International Symposium on Low Power Electronics and Design*, Seoul, Korea, pp. 134-139, August 2003.
- C32. F. Li, D. Chen, L. He, and J. Cong, "Architecture Evaluation for Power-Efficient FPGAs," *ACM/SIGDA International Symposium on FPGA*, Monterey, California, pp. 175-184, February 2003.
- C33. D. Chen, J. Cong, M. Ercegovac, and Z. Huang, "Performance-Driven Mapping for CPLD Architectures," *ACM/SIGDA International Symposium on FPGA*, Monterey, California, pp. 39-47, February 2001.
- C34. D. Chen, R. Colwell, H. Gelman, P. K. Chrysanthis, and D. Mosse, "A Framework for Experimenting with QoS for Multimedia Services," *International Conference on Multimedia Computing and Networking*, San Jose, California, January 1996.

Other Non-referred Workshop Papers or Poster Papers

- W1. L. Wan, C. Dong, and D. Chen, "A New Coarse-Grained Reconfigurable Architecture with Fast Data Relay and Its Compilation Flow," *Symposium on Application Accelerators in HPC*, July 2009. (Three-page poster paper.)
- W2. A. Papakonstantinou, K. Gururaj, J. Stratton, D. Chen, J. Cong, and W.M. Hwu, "High-Performance CUDA Kernel Execution on FPGAs," *International Conference on Supercomputing*, June 2009. (Two-page extended abstract.)
- W3. C. Dong, S. Chilstedt, and D. Chen, "Variation Aware Routing for Three-Dimensional FPGAs," *Workshop on 3D Integration and Interconnect-Centric Architectures*, Feb. 2009. (A later version with the same title appeared in *IEEE Computer Society Annual Symposium on VLSI*, May 2009.)

University Services

- Member of Teaching Evaluation and Awards Committee, 2005-2007
- Graduate ECE Seminar Committee, 2006-2007
- Graduate Committee, 2007-2009
- CSL Policy and Planning Committee, 2008-2009
- Computer Engineering Committee, 2008-2009
- Ph.D. committee (prelims and/or final exams):
 Dr. Smruti R. Sarangi (CS, UIUC), Dr. Liang Deng (ECE, UIUC), Dr. Lei Cheng (CS, UIUC), Dr. Yu Zhong (ECE, UIUC), Mr. Sain-Zee Ueng (ECE, UIUC), Dr. Yidnek Mekonnen (ECE, UIUC), Dr. Zhiguo Qian (ECE, UIUC), Dr. Radu Teodorescu (CS, UIUC), Mr. Brian Greskamp (CS, UIUC), Mr. Rodolfo Pellizoni (CS, UIUC)

Invited Talks

Title	Conference or Seminar	Location	Year
Design and Synthesis for Low-Power		Altera Corp., San Jose	2005

FPGAs			
VLSI design: turning your big ideas into reality	ECE 200: Undergraduate Seminar	UIUC	2006
Technology Mapping Algorithms for Programmable Logic Devices	ECE 500: Graduate Seminar	UIUC	2006
Abstraction beyond RTL for Low-Power	Computer Engineering Seminar	UIUC	2006
Design and Synthesis for Low-Power FPGAs		Velogix Inc., San Jose	2006
3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	ECE 590B: Electromagnetics, Optics & Remote Sensing Seminar	UIUC	2007
System, Behavioral, and Logic Level Design Automation		T.J. Watson Research Center, IBM	2007
3D nFPGA: A Three Dimensional CMOS/Nanomaterial Hybrid FPGA Architecture	Computer Engineering /Circuits Seminar	UIUC	2007
3D nFPGA: A CMOS/Nanomaterial Hybrid Reconfigurable Architecture	Workshop on SoC Design Methodologies	Seoul National University, Seoul, Korea	2007
Design and Synthesis for Low-Power FPGAs		Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China	2007
New Design Techniques and Architectures for FPGAs		University of Toronto, Toronto, Canada	2008
New Design Techniques and Architectures for FPGAs		Altera Corp., Toronto	2008
New Design Techniques and Architectures for FPGAs		Xilinx Corp., Toronto	2008
EPOS: an Explicitly Parallel Operations System	Workshop of SoC Design Methodologies	National Tsing Hua University, Taiwan	2008
New Synthesis and Architecture Solutions for Reconfigurable ICs	DLP and VLSI/CAD Workshop	National Tsing Hua University, Taiwan	2008
New Synthesis and Architecture Solutions for Reconfigurable ICs		National Taiwan University, Taiwan	2008
Variation-Aware Chip Design for Reliability and Performance		Sun Microsystems, Inc.	2008
Reconfigurable Circuits Design with Nanomaterials	Design, Automation and Test in Europe (DATE)	Nice, France	2009
New Binding Algorithms for Glitch and Inter-transition Power Reduction	An ECSI and USB Workshop on High Level Synthesis: Next Step to Efficient ESL Design	Yokohama, Japan	2009
Nano 3D FPGAs: Design and CAD		T.J. Watson Research Center, IBM	2009
Design and CAD for Nanoscale Reconfigurable Logic		Stanford University	2009

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